NOTE: Page numbers for previous revisions may differ from page numbers in the current version

Revision 1.0: Released to Market

PART NUMBER	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT81625QMTDR	Tape & Reel	4000	1625Q	8	8-Lead 3mm×3mm Plastic MSO

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V_{IN}=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		2.92		50	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising		2.9 160		V mV
I_{SD}	Shutdown current	$V_{FA/SYCN/SD}$=5V		3.7	8	uA
I_Q	Quiescent current from VIN	no load, no switching		460		uA
Reference and Control Loop						
V_{REF}	Reference voltage of FB	Tj=25°C	1.241	1.26	1.278	V
		Tj=-40~125°C	1.222		1.297	
I_{FB}	FB pin leakage current	V_{FB}=1V			100	nA
G_{EA}	Error amplifier trans-conductance	V_{COMP}=1.5V	500	700	900	uS
I_{COMP_SRC}	Error amplifier maximum source current	V_{FB}=V_{REF}-200mV, V_{COMP}=1.5V	120	155	195	uA
I_{COMP_SNK}	Error amplifier maximum current	V_{FB}=V_{REF}+200mV, V_{COMP}=1.5V	-170	-130		

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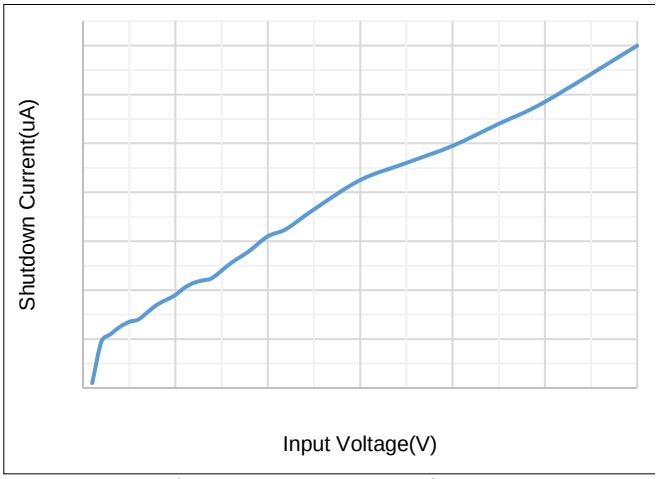

Figure 1. ISD vs Input Voltage

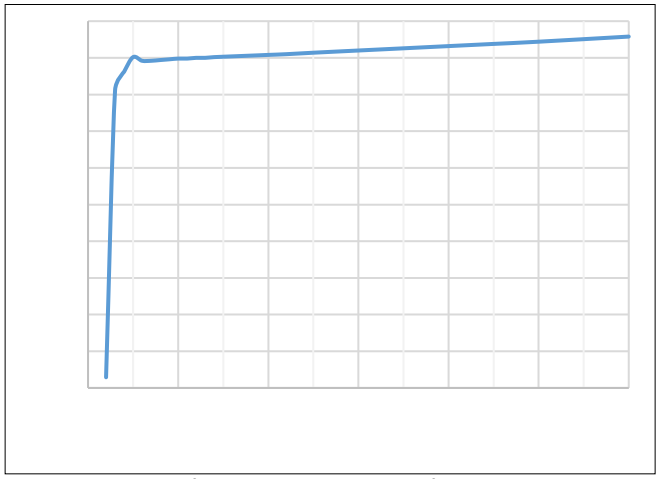

Figure 2. IQ vs Input Voltage

Figure 3. Switching Frequency vs RT

Figure 4. Switching Frequency vs Temperature

Figure 5. Efficiency vs Load Current, Boost, VOUT=12V

Figure 6. Efficiency vs Load Current, Sepic, VOUT=12V

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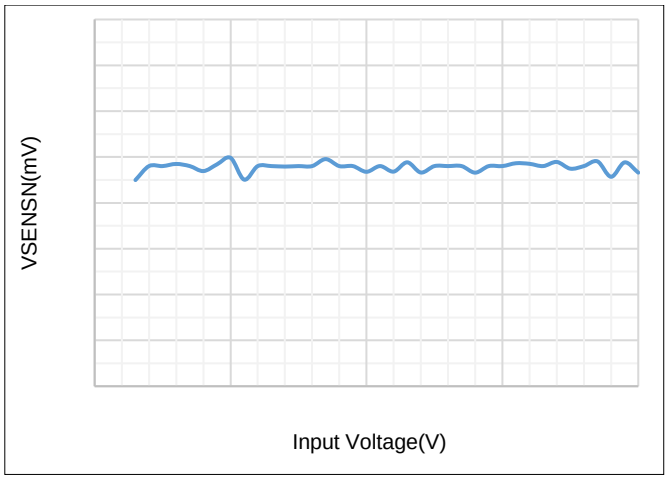

Figure 7. VSENSN vs Input Voltage

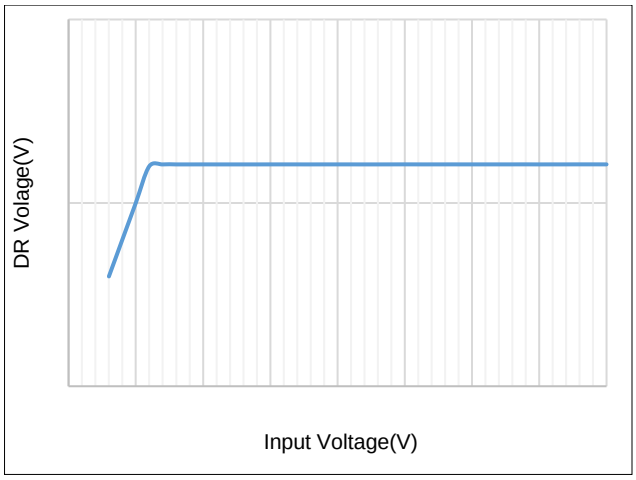

Figure 8. DR Volage vs Input Voltage

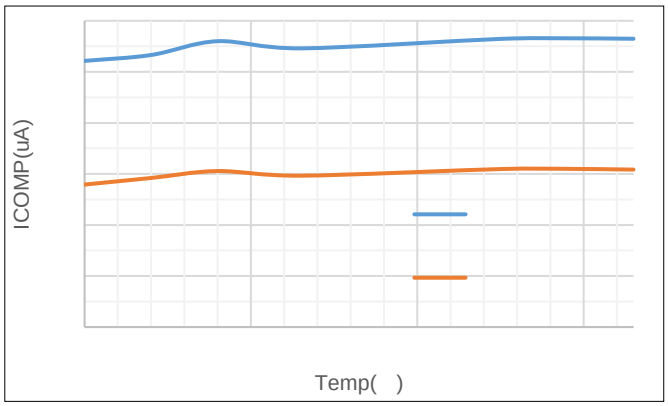

Figure 9. COMP Current vs Temperature

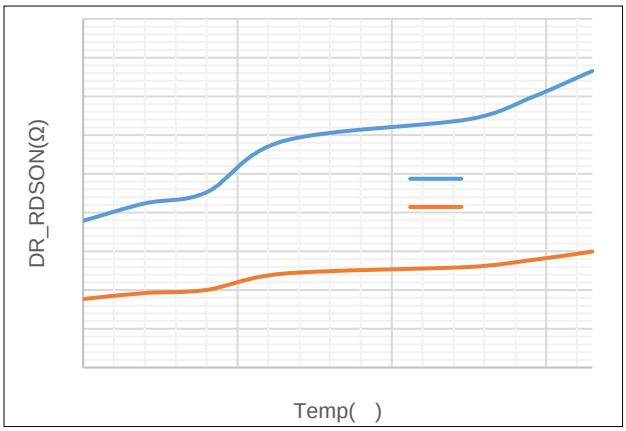

Figure 10. DR Resistance vs Temperature

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The current mode control scheme samples the inductor current, IL, and compares the sampled signal, Vsamp, to a internally generated control signal, Vc. The current sense resistor, RSEN, as shown in Figure11 converts the sampled inductor current, IL, to the voltage signal, Vsamp, that is proportional to IL such that

$$V_{samp} \quad I_L * R_{SEN} \tag{1}$$

Figure12 illustrate the theory why Sub-Harmonic Oscillation happen, the rising and falling slopes, M1 and -M2 respectively, of Vsamp are also proportional to the inductor current rising and falling slopes, Mon and -Moff respectively. Where Mon is the inductor slope during the switch on-time and -Moff is the inductor slope during the switch off-time and are related to M1 and -M2 by

$$M_1 \quad M_{on} * R_{SEN} \tag{2}$$

$$M_2 \quad M_{off} * R_{SEN} \tag{3}$$

For the boost topology:

$$M_1 \quad M_{on} * R_{SEN} \quad Vin * R_{SEN} / L \tag{4}$$

$$M_2 \quad M_{off} * R_{SEN} \quad (Vout \quad Vin) * R_{SEN} / L \tag{5}$$

In Figure10, a small increase in the load current causes the sampled signal to increase by ΔVsamp0. The effect of this load change, ΔVsamp1, at the end of the first switching cycle is

$$'V_{samp1} \quad (\frac{M_2 \quad M_c}{M_1 \quad M_c}) * 'V_{samp0} \tag{6}$$

So, When No compensation ramp signal is added, which Mc is zero, then:

$$'V_{samp1} \quad (\frac{M_2}{M_1}) * 'V_{samp0} \quad (\frac{D}{1 \quad D}) * 'V_{samp0} \tag{7}$$

When D > 0.5, ΔVsamp1 will be greater than ΔVsamp0. In other words, the disturbance is divergent. So a very small perturbation in the load will cause the disturbance to increase.

After a compensation ramp is added to the control signal. To ensure that the perturbed signal converges we must maintain:

$$\left| (\frac{M_2 \quad M_c}{M_1 \quad M_c}) \right| < 1 \tag{8}$$

The compensation ramp has been added internally in the SCT81625Q. The slope of this compensation ramp has been selected to satisfy most applications, and it's value depends on the switching frequency. This slope can be calculated using the formula:

$$M_c \quad V_{SL} * F_s \tag{9}$$

VSL is the amplitude of the internal compensation ramp and FS is the controller's switching frequency.

For more flexibility, slope compensation can be increased by adding one external resistor, RSL, in the ISEN's path. Figure13 shows the setup. The externally generated slope compensation is then added to the internal slope compensation of the SCT81625Q. When using external slope compensation, the formula for Mc becomes:

$$M_c \quad (V_{SL} \quad K * R_{SL}) * F_s$$

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Typical Application (Boost)

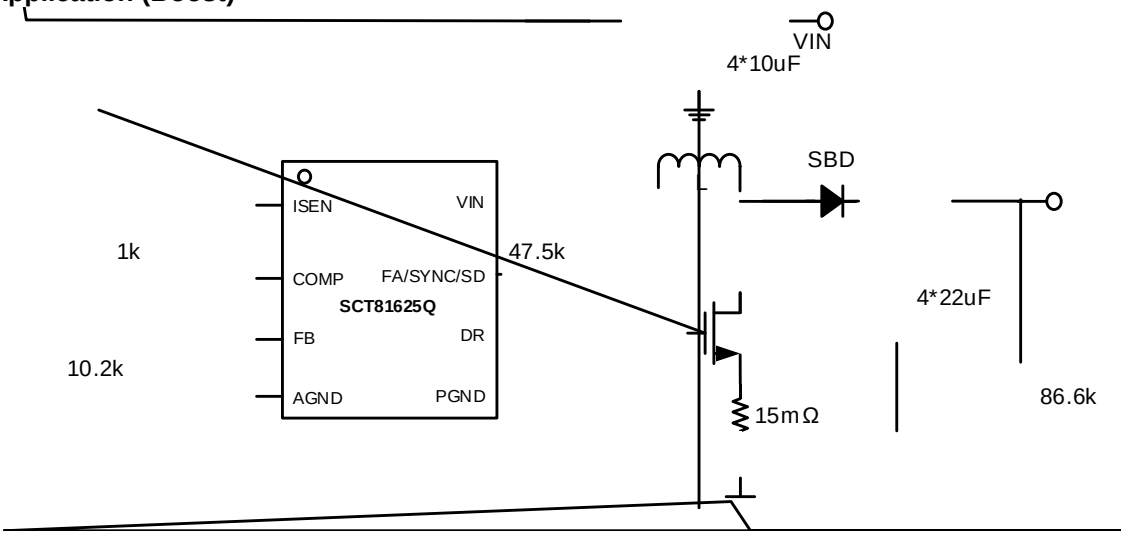

Figure 18. Application Schematic, 3V to 11V, 2A Boost Regulator at 400kHz

Design Parameters

Design Parameters	Example Value
Input Voltage	5V Normal 3V to 11V
Output Voltage	12V
Maximum Output Current	3A
f1witching Frequency	

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Inductor Selection (Boost)

The performance of inductor affects the power supply's steady state operation, transient behavior, loop stability, and boost converter efficiency. The inductor value, DC resistance, and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DC resistance, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have ±20% or even ±50% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, maxim load current and minimum switching frequency of the application, while considering the inductance with -

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chosen in the r e ʏ O tʏ ˢ O M̌ Ҡ ⁄ Mʎ eп ⁑ n is ª then

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I_G is the gate drive current.

The total power dissipation of MOSFET includes conduction loss as shown in the first term and switching loss as

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Application Waveforms

Vin=5V, Vout=12V, unless otherwise noted

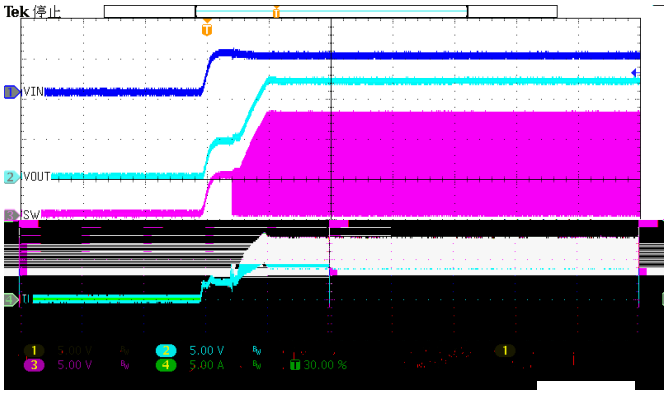

Figure 19. Power up(Iload=2A)

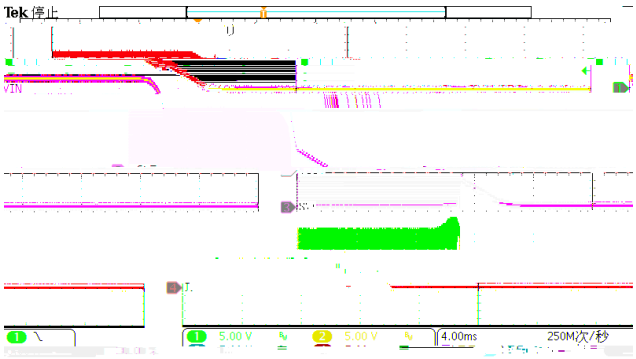

Figure 20. Power down(Iload=2A)

Figure 21. Over current protection (Iload=5A)

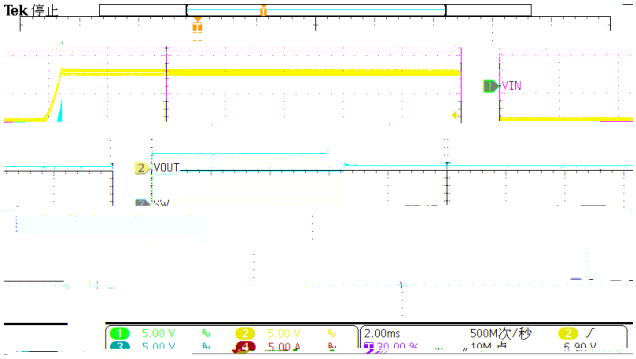

Figure 22. Over current recovery (Iload=5A)

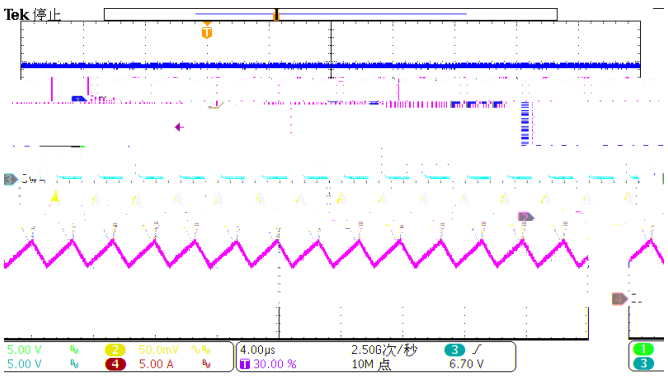

Figure 23. Steady-state (Iload=2A)

Figure 24. Sync Frequency

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Typical Application (S

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Inductor Selection (Sepic)

A good rule

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The total power dissipation of MOSFET includes conduction loss as shown in the first term and switching loss as shown in the second term. The total power dissipation should be within package thermal ratings.

Output Diode Selection

The diode at the output side must withstand the reverse voltage when the MOSFET is turned-on. The peak reverse voltage is given by:

$$V_{D\_PEAK} \quad V_{IN\_MAX} \quad V_{O\_MAX} \tag{35}$$

The diode should also be capable to flow switch peak current IQ_PEAK.

The power dissipation of the diode is equal to the forward voltage drop multiplies output current. Schottky diodes are recommended here to minimize the power loss.

Coupling Capacitor Selection

For ceramic capacitors with low-ESR, the peak to peak voltage ripple on coupling capacitor is estimated by:

$$V_{CS}' \quad \frac{I_O \ \mathrm{u} D_{MAX}}{C_S \ \mathrm{u} f_{SW}} \tag{36}$$

The maximum voltage across the coupling capacitor is maximum input voltage. The voltage rating of the coupling capacitor must be greater than it.

The RMS current of coupling capacitor is given by:

$$I_{CS\_RMS} \quad I_O \quad \sqrt{\frac{V_O \ \mathrm{u} V_D}{V_{IN\_MIN}}} \tag{37}$$

There is a large RMS current through coupling capacitor relative to output power. Ensure the coupling capacitor can withstand it with good heat generation to have proper thermal performance.

Input Capacitor Selection

The SEPIC has an inductor at input side thus the input current is continuous and triangular. The RMS current flowing through the input capacitor is given by:

$$I_{IN\_RMS} \quad \frac{'I_{L1}}{\sqrt{12}} \tag{38}$$

Since input current ripple is relative low, the capacitance would be not too critical. While 100μF in total or higher value is strongly recommended in order to provide stable input supply.

Output Capacitor Selection

Similar to boost converter, the SEPIC output capacitor suffers large current ripple. The capacitance must be enough to provide the load current. The maximum voltage ripple in the output capacitor is:

$$'V_{OUT} \quad \frac{I_O \ \mathrm{u} D_{MAX}}{C_{OUT} \ \mathrm{u} f_{SW}} \quad ESR \ \mathrm{u} \ I_{L1\_PEAK} \quad I_{L2\_PEAK} \tag{39}$$

Assuming ceramic capacitors are used here and ESR can be ignored, the output capacitor is given by:

$$OUT \quad \frac{O \qquad MAX}{OUTOUTu} \tag{40}$$

The output capacitor must have a enough RMS current rating to handle the maximum RMS current in the output capacitor, calculated by:

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$$I_{COUT\_RMS} \quad I_O \quad \sqrt{\frac{D_{MAX}}{1 \quad D_{MAX}}} \qquad (41)$$

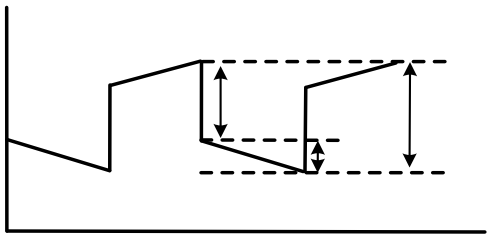

Figure 26. Output Voltage Ripple

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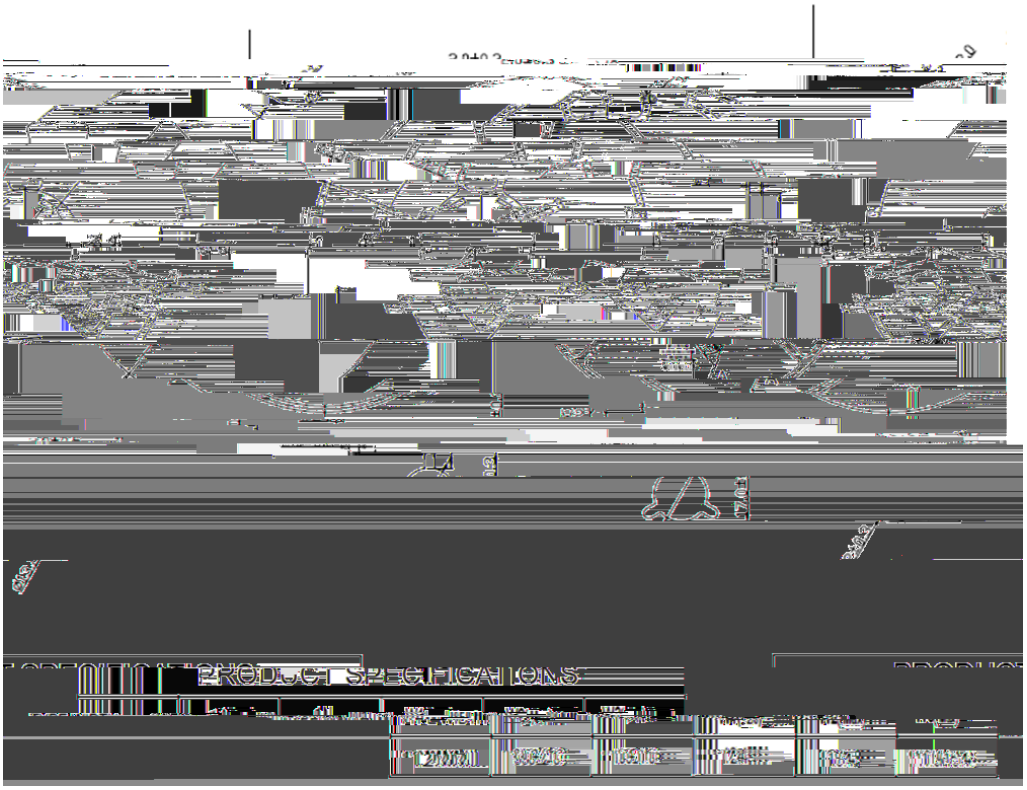

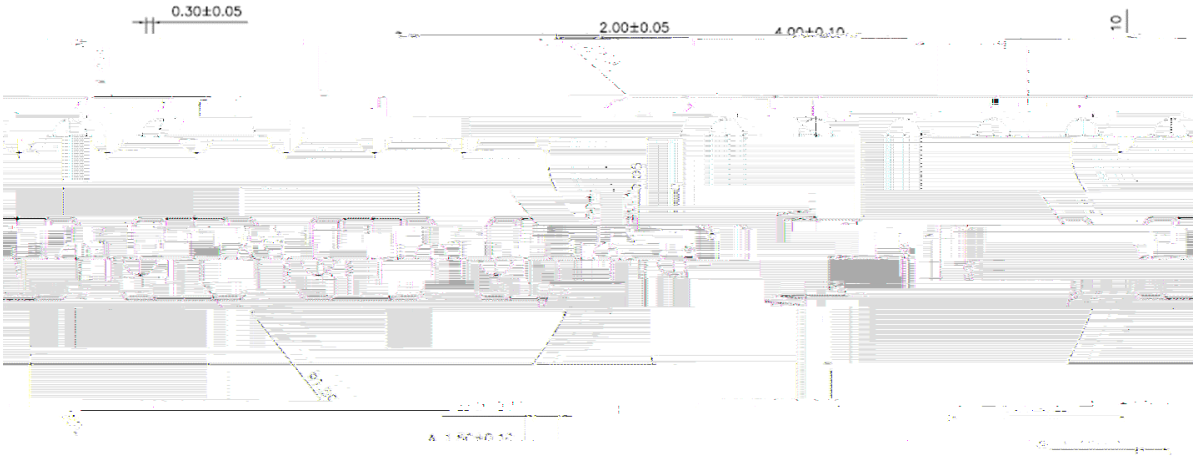

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