N~

Wide Input Voltage: 4.2-17V
3A Continuous Output Current with Integrated

EMC /Span <MCID 47/Lang (en-US)>BDC q0.00000912 0 612 792 reW* nBT/F3 9.96 Tf1 0 0 1 1835.1 655632 6m0 q0 GR]TJE

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Released to Market
Revision 1.1: Correct package information
Revision 1.2: Update PACKAGE INFORMATION(SOT563)
Revision 1.3: Update DEVICE ORDER INFORMATION
Revision 1.4: Update ABS T

NAME	NO.	PIN FUNCTION
GND	1	Power ground. Must be soldered directly to ground plane.
SW	2	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BST to power the high-side switch.
VIN	3	Power supply input. VIN supplies the power to the IC, as well as the step-down converter switches. Drive VIN with a 4.2V to 17V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC. See Input Capacitor.
FB	4	Buck converter output feedback sensing voltage. Connect a resistor divider from VOUT to FB to set up output voltage. The device regulates FB to the internal reference of 0.8V typical.
EN	5	Enable logic input. Floating the pin enables the device. The device has precision enable thresholds 1.2V rising / 1.1V falling for programmable UVLO threshold and hysteresis.
BST	6	Power supply for the high

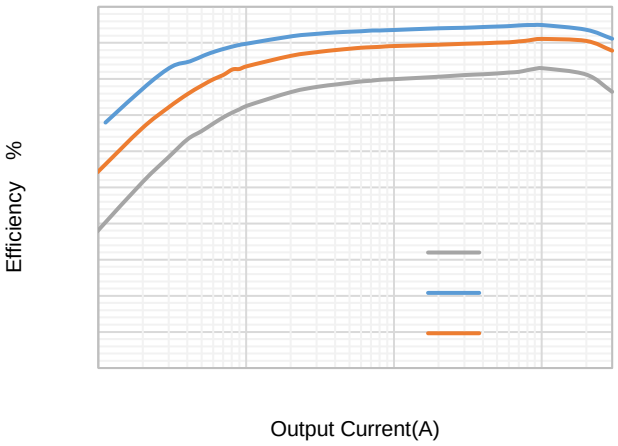


Figure 1. SCT2230C Efficiency, Vin=12V

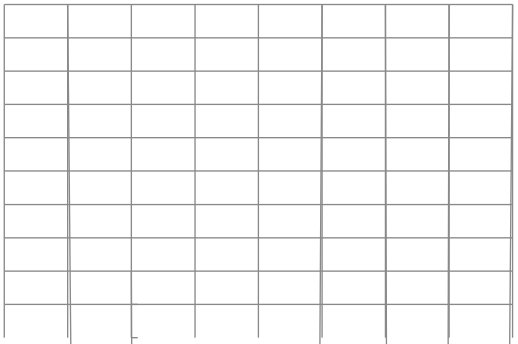


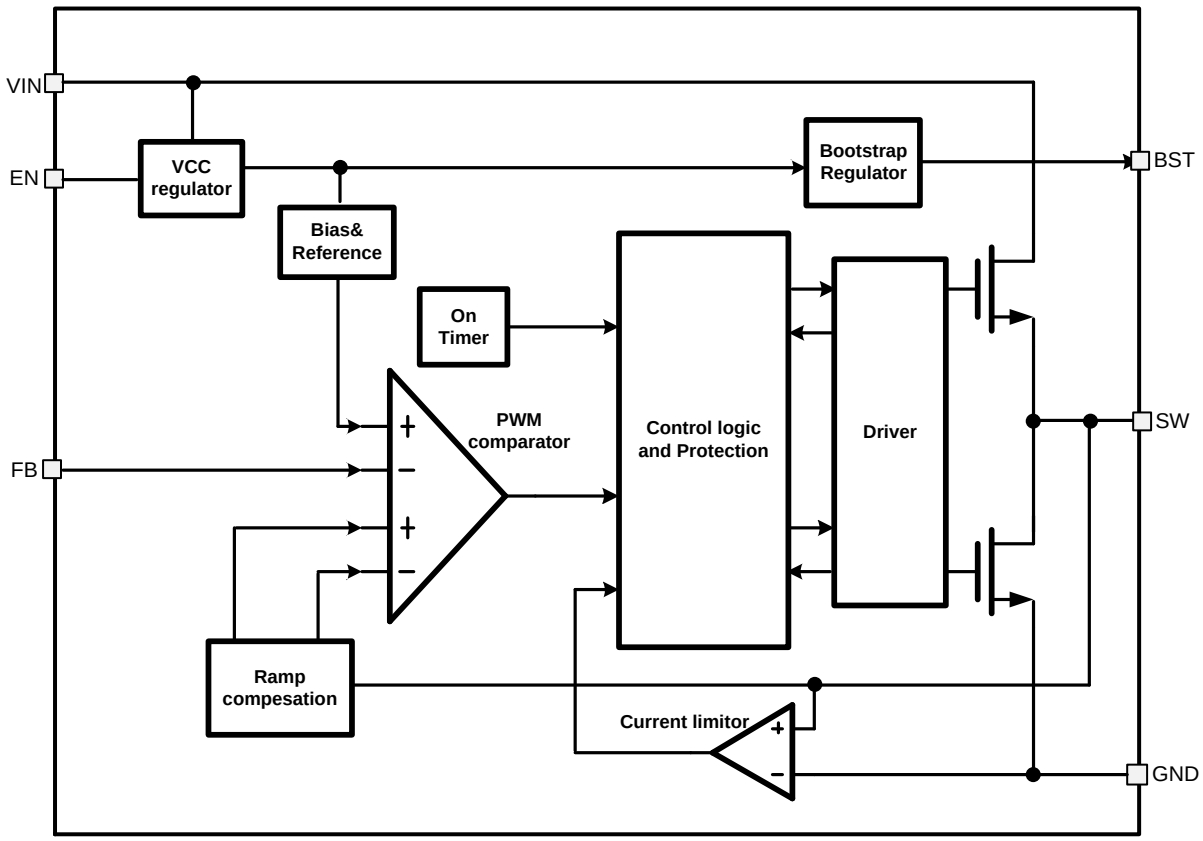
Figure 2. UVLO Vs. Temperature

Figure 3. Line Regulation

Figure 4. Load Regulation

Figure 5. Feedback Voltage vs. Temperature

Figure 6. Quiescent Current vs. Temperature


VIN
EN
FB
VCC regulator
Bias& Reference
Bootstrap Regulator
BST
On Timer
PWM comparator
Control logic and Protection
Driver
SW
Ramp compesation
Current limitor
GND

Under Voltage Lockout UVLO

The SCT2230C Under Voltage Lock Out (UVLO) default startup threshold is typical 3.9V with VIN rising and shutdown threshold is 3.6V with VIN falling. The more accurate UVLO threshold can be programmed through the precision enable threshold of EN pin.

Enable and Start up

When applying a voltage higher than the EN high threshold (typical 1.2V/rise), the SCT2230C enables all functions and the device starts soft-start phase. The SCT2230C has the built in 2.5ms soft-start time to prevent the output overshoot and inrush current. When EN pin is pulled low, the internal SS net will be discharged to ground. Buck operation is disabled when EN voltage falls below its lower threshold (typically 1.1V/fall).

An internal 1.5uA pull up current source connected from internal LDO power rail to EN pin guarantees that floating EN pin automatically enables the device. For the application requiring higher VIN UVLO voltage than the default setup, there is a 5.3uA hysteresis pull up current source on EN pin which configures the VIN UVLO voltage with an off-chip resistor divider R3 and R4, shown in Figure 7. The resistor divider R3 and R4 are calculated by equation (3) and (4).

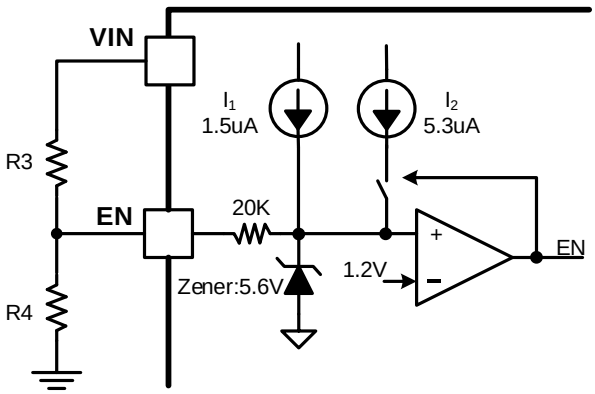


Figure 7. Adjustable VIN UVLO

Over Current Protection (OCP) and Hiccup Mode

In each switching cycle, the inductor current is sensed by monitoring the low-side MOSFET during the OFF period. When the voltage between GND pin and SW pin is lower than the over current threshold voltage, the OCP will be triggered and the controller keeps the OFF state. A new switching cycle will begin only when the measured voltage is higher than limit voltage. If output loading continues to increase, output will dropped below the UVP, and SS pin is discharged such that output is 0V. Then the device will count for 7 cycles of soft-start time for hiccup waiting time and restart normally after 7 cycles soft-start period.

Bootstrap Voltage Regulator

An external bootstrap capacitor between BST and SW pin powers floating high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

Thermal Shutdown

Once the junction temperature in the SCT2230C exceeds 160°C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 140°C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

Typical Application

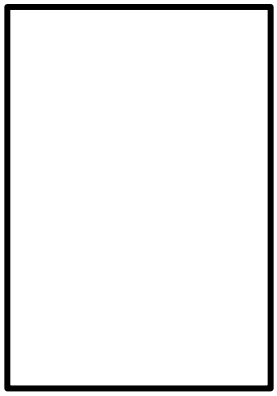


Figure 8. 12V Input, 3.3V/3A Output

Design Parameters

Design Parameters	Example Value
Input Voltage	12V
Output Voltage	3.3V
Output Current	3A

S1S1S1S1S1S1S1S1S1S1

ripple less than 100mV. Generally, a 25V/10uF input ceramic capacitor is recommended for most applications. Choose the right capacitor value carefully with considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

Inductor Selection

The performance of inductor affects the power supply's steady state operation, transient behavior, loop stability, and buck converter efficiency. The inductor value, DC resistance (DCR), and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DCR, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Cho

Layout Guideline

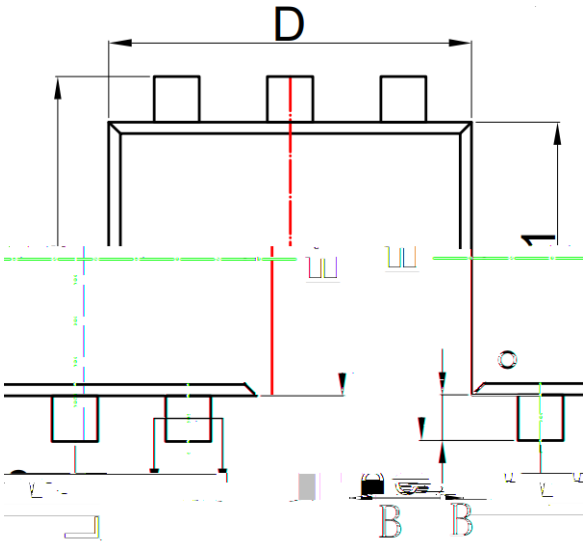
The regulator could suffer from instability and noise problems without carefully layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be very close to the VIN pin and GND pin to reduce the input supply ripple. Place the capacitor as close to VIN pin as possible to reduce high frequency ringing voltage on SW pin as well. Figure 15

TSOT23-6L TOP VIEW

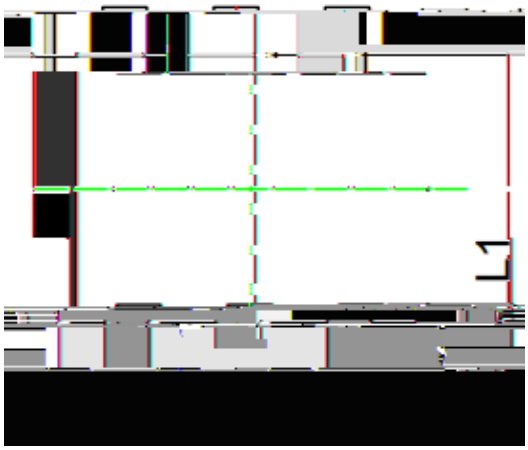
TSOT23-6L SIDE VIEW

NOTE:

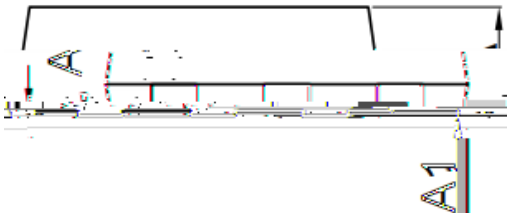
1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.



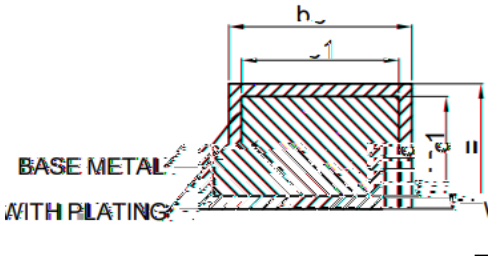
SOT563 TOP VIEW



SOT563 BOTTOM VIEW



SOT563 SIDE VIEW

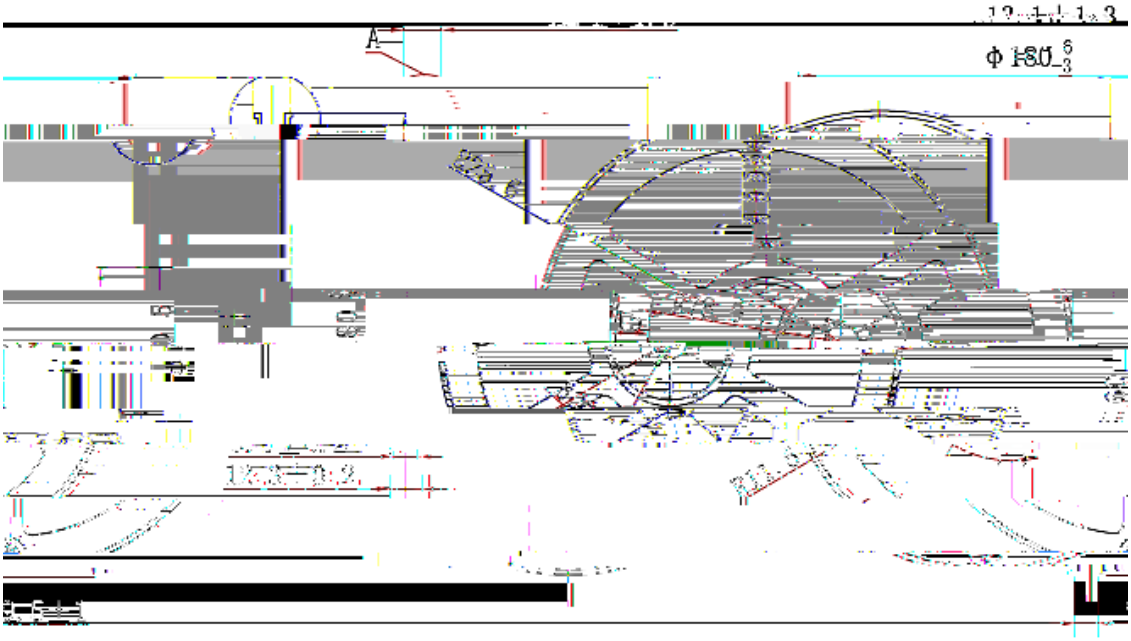


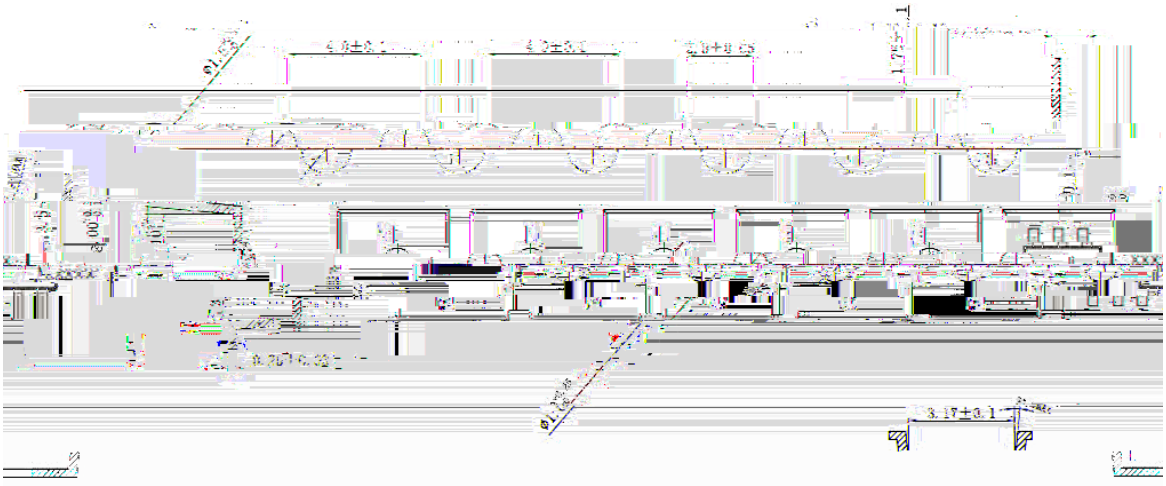
SECTION B-B

NOTE:

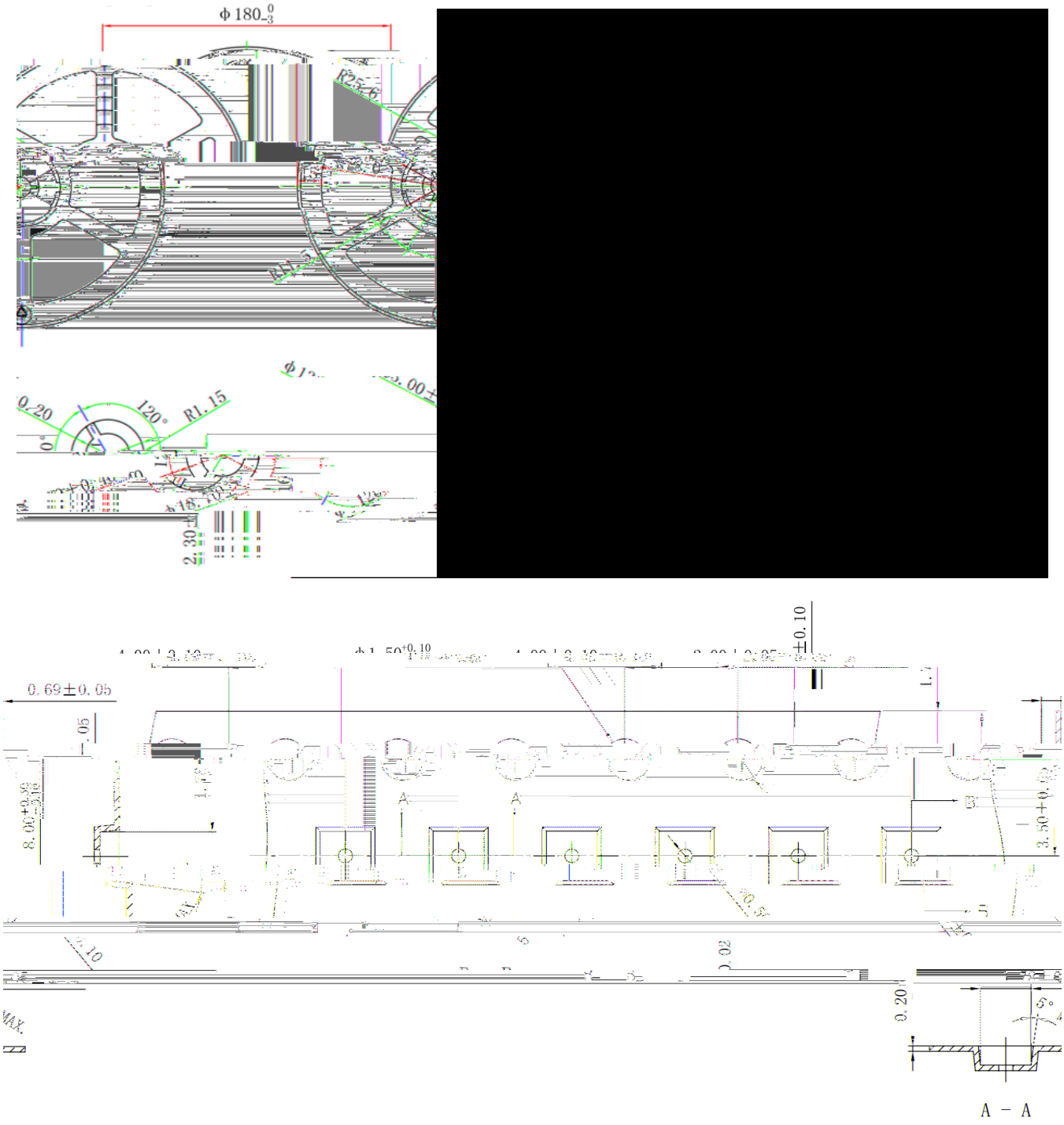
7. Drawing proposed to be made a JEDEC package outline MO-220 variation.
8. Drawing not to scale.
9. All linear dimensions are in millimeters.
10. Thermal pad shall be soldered on the board.
11. Dimensions of exposed pad on bottom of package do not include mold flash.
12. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	0.53	---	0.60
A1	0.00	---	0.05
b	0.19	---	0.27
b1	0.18	0.20	0.23
c	0.11	---	0.16
c1	0.10	0.11	0.12
D	1.50	1.60	1.70
E	1.503	1.60	1.70
E1	1.10	1.20	1.30
e	0.50BSC		
L	0.10	0.20	0.30
L1	0.20	0.30	0.40





Feeding Direction


Φ180
R25.6
R1.15
120°
0.69±0.05
±0.10
A – A
Feeding Direction